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| 10/711,978 | 10/18/2004 | Paul H. Bergeron | BUR920040134US1 | 5977 |

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| EXAMINER |
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WHITMORE, STACY

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| ART UNIT | PAPER NUMBER |
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2825

| SHORTENED STATUTORY PERIOD OF RESPONSE | NOTIFICATION DATE | DELIVERY MODE |
|--|-------------------|---------------|
| 3 MONTHS | 01/31/2007 | ELECTRONIC |

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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gbpatent@gbpatent.com
pto@gbpatent.com

Office Action Summary

Application No.

10/711,978

Applicant(s)

BERGERON ET AL.

Examiner

Stacy A. Whitmore

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 October 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 October 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 10/04, 11/04.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application
- ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The limitation of claim 4 is already disclosed in the locating step of claim 1.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 2-3, 5, 7, 9-10, and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

I. As for claims 2-3, and 10, the term Mx and Mx-1 are unclear because it is not clear from either the claim language or the specification exactly what the MX layer is. For example, in applicant's specification in paragraphs 35 and 36, the Mx layer may be either wires, wiring layers, or trenches. Clarify.

II. Claims 2, 5, 7 and 9 recite the limitation "implementing.....to a ground-rule" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

III. Claim 29, recites the limitation "the adjustable shape" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-30 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

4. As for claims 1-30, applicant claims methods modifying circuit design source data, and circuit design source data that all appear to be directed to the alteration of data, however, the steps such as implementing, widening, etc. do not appear to claim a physical alteration of data within a system. Further, claims 1-30 do not appear to produce a concrete, tangible, and useful result.

See M.P.E.P 2106 [R-5] Section IV. DETERMINE WHETHER THE CLAIMED INVENTION COMPLIES WITH 35 U.S.C. 101.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5, 9, 11-13, 16, 18-20, 23, and 25-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Su, J.Z., et al., "Post-route optimization for

improved yield using a rubber-band wiring model". Su was cited by applicant on the IDS dated November 12, 2004.

6. As for the claims, Su discloses the invention as claimed, including:

[Claim 1] 1. A method of modifying circuit design source data of a three- dimensional structure for improving integrated circuit yield, comprising the steps of: spreading wires using a post-routing layout optimizer [abstract, pg. 702, section 2; pg. 704, section 3.]; locating a problem structure remaining after post-layout optimizing using a shapes-processing tool [abstract, pg. 702, section 2; pg. 704, section 3. – the problem structure are the spot defects]; and implementing at least one local modification to said three- dimensional structure to perform a fix-up process on the problem structure [abstract, pg. 702, section 2; pg. 704, section 3. – the local modification is the spreading of the wires located over the spot defects];

[Claim 2] 2. The method of claim 1, wherein implementing at least one local modification to a ground-rule to perform a fix-up process comprises increasing the flexibility of at least one wire of an Mx layer passing over an incompatible structure component of the problem structure [pg. 701, figs. 1-2, and left hand side – the flexibility of the wire is provided by the rubber-band updating];

[Claim 3] 3. The method of claim 2, wherein increasing the flexibility of at least one wire comprises inserting at least one jog in the at least one wire [pg. 701, figs. 1-2, and left hand side – the flexibility of the wire is provided by the rubber-band updating, and the jog is the movement of the wire by the rubber-band process];

[Claim 4] 4. The method of claim 1, further comprising locating a problem structure using a shapes-processing tool [pg. 702, section 2. – the location of the defects is the location of a problem structure which must use some sort of shape processing tool in order to detect defects in materials];

[Claim 5] 5. The method of claim 1, wherein implementing at least one local modification to a ground-rule to perform a fix-up process comprises increasing a space-between at

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least two wires on a layer over an incompatible structure component of the problem structure [abstract, pg. 702, section 2; pg. 704, section 3. – the local modification is the spreading of the wires located over the spot defects];

[Claim 9] 9. The method of claim 1, wherein implementing at least one local modification to a ground-rule to perform a fix-up process comprises causing a router to reroute at least one wire [abstract, pg. 702, section 2; pg. 704, section 3. – the local modification is the spreading of the wires located over the spot defects, further pg. 702, first full paragraph shows the SURF tool as a router which uses the rubber-band wiring or re-routing];

[Claim 11] 11. A method of modifying circuit design source data for forming a multi-layer structure of a semiconductor device, comprising the steps of:
determining whether at least two minimum-spaced wires of an upper layer pass over a dishing-prone structure of a lower layer [abstract, pg. 702, section 2; pg. 704, section 3. – the local modification is the spreading of the wires located over the spot defects, the dishing prone structure is the structure that would leave the spots of missing material on the wafer]; and

if so performing at least one of:

increasing a space between the two minimum-spaced wires of the upper layer in a region over the dishing-prone structure of the lower layer [section 2; pg. 704, section 3.];
forming a dummy hole in a wide wire under the space between the two minimum-spaced wires; and widening a trench between two wide wires under the space between the two minimum-spaced wires [];

Note that the “if so” limitation of claim 11 inherently includes the “if not” situation, and therefore, the increasing and forming steps are not required by the claim language.

[Claim 12] 12. The method of claim 11, further comprising increasing the flexibility of at least one wire of the two minimum-spaced wires above the dishing-prone structure [see as cited in the rejection of claim 2];

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[Claim 13] 13. The method of claim 12, wherein increasing the flexibility of the at least one wire of the two minimum-spaced wires comprises forming at least one jog in the at least one wire [see as cited in the rejection of claim 3];

[Claim 16] 16. The method of claim 11, further comprising causing a router to reroute at least one wire of the at least two minimum-spaced wires [see as cited in the rejection of claim 9];

[Claim 18] 18. A method of modifying circuit design source data of a three-dimensional structure for forming a multi-layer structure of a semiconductor device, comprising the steps of:

forming a dishing-prone structure on a lower layer [pg. 702, section 2, the dishing prone structure is the structure causing the missing material on the wafer];

forming two minimum-spaced wires over the dishing-prone structure on an upper layer [pg. 704, section 3]; increasing a space between the two minimum-spaced wires in a region over the dishing-prone structure [pg. 704, section 3];

Note that the “if” claim language inherently includes the “if not” situation, and therefore the claim language as part of the “if” situation is not required to be rejected.

if the dishing-prone structure includes a wide wire, inserting a space for a dielectric island in the wide wire under at least one wire of the two minimum-spaced wires; and
if the dishing-prone structure includes a narrow trench between two wide wires, widening the narrow trench under of the space between the two minimum-spaced wires
[];

[Claim 19] 19. The method of claim 18, further comprising increasing the flexibility of at least one wire of the two minimum-spaced wires proximate the dishing-prone structure [see as cited in the rejection of claim 2];

[Claim 20] 20. The method of claim 19, wherein increasing the flexibility of the at least one wire comprises forming at least one jog in the at least one wire of the two minimum-spaced wires [see as cited in the rejection of claim 3];

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[Claim 23] 23. The method of claim 18, further comprising causing a router to reroute at least one wire of the at least two minimum-spaced wires [see as cited in the rejection of claim 9];

[Claim 25] 25. Circuit design source data for a multi-layer structure of a semiconductor device, comprising:

an upper layer comprising multiple minimum-spaced wires [pg. 702, section 2.; pg. 704, section 3];

a lower layer comprising a dishing-prone structure, wherein the multiple minimum-spaced wires of the upper layer are disposed over the dishing-prone structure of the lower layer [pg. 702, section 2.; pg. 704, section 3]; an increased space between at least two wires of the multiple minimum-spaced wires in a region over the dishing-prone structure [pg. 702, section 2.; pg. 704, section 3];

Note that the "if" claim language inherently includes the "if not" situation, and therefore the claim language as part of the "if" situation is not required to be rejected.

a dummy hole in the wide wire under at least one wire of the multiple minimum-spaced wires if the dishing-prone structure includes a wide wire; and a widened region of the narrow trench under at least one wire of the multiple minimum-spaced wires if the dishing-prone structure includes a narrow trench between two wide wires [];

[Claim 26] 26. The circuit design data of claim 25, comprising a jog in at least one wire of the multiple minimum-spaced wires proximate the dishing-prone structure [see as cited in the rejection of claim 3];

[Claim 27] 27. The circuit design data of claim 26, comprising at least two jogs in at least one wire of the multiple minimum-spaced wires proximate the dishing-prone structure [see as cited in the rejection of claim 3];

[Claim 28] 28. The circuit design data of claim 25, wherein an increased space between at least two wires of the multiple minimum-spaced wires comprises an adjustable shape between the at least two wires of the multiple minimum-spaced wires [pg. 701, figs. 1-2,

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the adjustable shape as claimed may just be the shape that is between the wires and not necessarily another entity between the wires];

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stacy A Whitmore

Primary Examiner

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SAW

January 23, 2007

A handwritten signature in black ink, appearing to read 'SAW' followed by a stylized flourish.